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# FABRICATION AND STUDY OF THE $p-\mathrm{Si}/\alpha-\mathrm{Si}/\mathrm{Ag}$ MEMRISTOR CROSSBAR ARRAY

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We study the formation of the conductive channels in $\alpha$-Si memristors and demonstrate their operation in the crossbar array. The latter can be utilised as the basic component of the neuromorphic chip tailored for edge computing. The conductive channels in $\alpha$-Si are formed by the migration of Ag along with Cu ions. Such a channel has switching current-voltage characteristics at high bias, $V_{bias}$>2V, and highly non-linear that at low bias, $V_{bias}$<0.5V. Memristor can be re-programmed to different resistance states with short voltage pulses of amplitude above 2 V. We demonstrate the programming of the memristor crossbar array and its operation in vector-by-matrix multiplication with an 87% accuracy.

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## 1. INTRODUCTION

The concept of neuromorphic computing has evolved over the decades into an interdisciplinary field at the boundary between neuroscience and advanced computing [1]. Aiming to overcome the limitations of the von Neumann architecture, neuromorphic systems tend to exploit in-memory and parallel computing principles, which are crucially important for such intensively developing areas as edge computing, the Internet of Things, and machine learning [2]. Memristors, multilevel two-terminal storage devices, are considered one of the candidates for the hardware implementation of neuromorphic systems that enable parallel computing with low power consumption [3]. The ideal memristor should have re-programmable resistance states, strong non-linear current–voltage characteristics at low bias voltage, and a long retention time.

Typically, the core part of a memristor consists of two metal electrodes and an insulating layer in between, which serves as a switching and non-linear medium. A conductive channel can be formed by metal ions drifting under an applied electric field in the insulating layer [4]. When the electric field between the metal electrodes exceeds a threshold value, the metal ions diffuse into the insulating layer, where they form conductive channels. The conductive channels are prone to variations under external signals. Ideally, the variations should be done in a fully controllable way [5]. There is a wide range of insulating materials and metals used in the memristors, such as oxides, nitrides, selenides, perovskites, polymeric materials, amorphous silicon ($\alpha$-Si), Ag, Cu, Ti, etc. [1] However, a common problem, called the «tunability–stability dilemma» between the controllable tuning of resistance and its long-term stability, remains unsolved [6]. It arises because of the poor control of highly mobile metal ions. For instance, Ag conductive channels in $\alpha$-Si demonstrate a good switching capability due to the high mobility of Ag ions. However, its functionality is limited by the large stochasticity of the ion movement, which results in the low stability of conductive channels. Recently, Yeon et al. has shown that Cu can promote and stabilise Ag channels in $\alpha$-Si [7]. Cu ions make stable compounds with Si (silicides) and have good compati-

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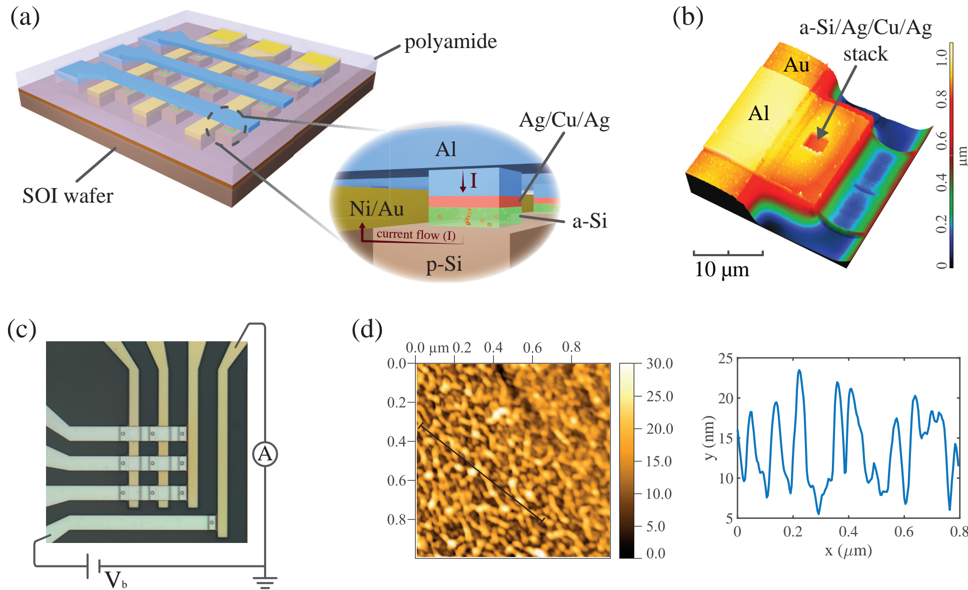


**Fig. 1.** Material composition of the $\alpha$-Si memristor with Ag/Cu conductive channels. $a$ — Layer-by-layer structure of the device. The Ni/Au electrodes contact the $p$-Si of the SOI wafer, whereas the Al electrodes contact the Ag/Cu layer. The conductive channel is formed in $\alpha$-Si by the diffusion of Ag and Cu ions. Polyamide insulates the bottom and top electrodes. $b$ — AFM image of the node of a memristor crossbar array. The conductive channel is formed in the polyamide window with $\alpha$-Si/Ag/Cu/Ag stack. $c$ — Optical microscope image of a 3×3 memristor crossbar array and one standalone memristor. A schematic of a *dc* measurement circuit is included, illustrating the application of a bias voltage $V_b$ across Au (bitline) and Al (wordline) electrodes. $d$ — AFM image of a 1-$\mu$m-thick $p$-Si prior to the deposition of $\alpha$-Si/Ag/Cu/Ag stack

bility with Ag. The authors have significantly improved the stability of resistance states and the repeatability of switching in $\alpha$-Si. Further improvement of the channel stability has been achieved by introducing a barrier layer of intrinsic silicon oxide ($i$-$SiO_x$) in between $\alpha$-Si and $p$-Si ($\rho$=0.001–0.005 $\Omega$·cm) [8]. This oxide exhibits Ag diffusivity comparable to that in $\alpha$-Si and on its own demonstrates reliable multilevel resisitve switching with high endurance [9–11]. At the same time, diffusivity of Cu in $i$-$SiO_x$ is lower [12]. Thus, a thin layer of $i$-$SiO_x$ may limit the motion of ions when stacked with $\alpha$-Si such that resistive switching occurs predominantly at the $\alpha$-Si/$i$-$SiO_x$ interface. However, despite the broad research done with $\alpha$-Si memristors, it is still not entirely clear what factors might influence filament stability of Ag/Cu filaments in $\alpha$-Si.

For the applications, the memristors are assembled into a crossbar array, see Fig. 1 $a$. Such an array can efficiently perform matrix operations, like vector-by-matrix multiplication and solving linear equations. It reduces the complexity of big data analysis problems from $\mathcal{O}(N^{3.5}) - \mathcal{O}(N^4)$ to pseudo-$\mathcal{O}(N)$ [13]. For such functionality, large-scale memristor crossbar arrays must fully meet the following requirements: (i) uniform digital and analogue switching with <1% spatial and temporal variation; (ii) stable analogue switching with linear and symmetrical up/down conductance update; and (iii) long retention time of each resistance state.

In this work, we study memristors made of Ag/Cu conductive filaments in $\alpha$-Si. When placed in contact with p-Si, the memristor behaves as a one-diode-one-memristor (1D1R) with an intrinsic current nonlinearity [14]. Here, the role of the diode is played by the Schottky barrier at the interface between $p$-Si and $\alpha$-Si. We explore both individual memristors and crossbar arrays of memristors. A stable channel is formed when the thickness of the $\alpha$-Si layer is 5 nm–10 nm. The bias voltage for the formation of the conductive channel is above 5 V. The resistance of the state can be altered with the programming voltage pulses of amplitude above 2 V and duration longer than 0.1 s.

For assessment of the technology, we demonstrate a product of a vector and a square 3×3 matrix. The analog result agrees with the expected values with 87% accuracy. The accuracy is limited by the presence of the sneak path currents in a crossbar array and arbitrary fluctuations of resistance.

## 2. EXPERIMENTS AND DISCUSSION

### 2.1. Fabrication of the memristors

The crossbar with the memristor is shown in Fig. 1 *a*. We start with the SOI wafer having a 5-$\mu$m-thick p-Si as the device layer ($\rho$=0.01–0.02 $\Omega$·cm) isolated from a bulk Si with a 2-$\mu$m-thick $SiO_2$ layer. The $p$-Si layer is thinned down to 0.8–1 $\mu$m with $SF_6$ plasma etching followed by fabrication of the 10-$\mu$m-wide Ni(10 nm)/Au(90 nm) wordlines. The overall contact resistance between p-Si and Au/Ni is below 3 $k\Omega$. The $p$-Si is then removed to isolate the wordlines from each other, and only 10×10 $\mu m^2$ $p$-Si stands for memristor stack are retained. The surface of the stands has a roughness of ∼5 nm, see Fig. 1 *d*. The stacks of $\alpha$-Si(5–10 nm)/Ag(3 nm)/Cu(3 nm)/Ag(15 nm) are deposited on the stands during the next fabrication step. The top Al (120 nm) electrodes, or the wordlines, are fabricated over the stack perpendicular to the bitlines. The Au/Ni and Al lines are isolated from each other with the 500-nm-thick polyamide. The polyamide also covers the $p$-Si stands, and only windows of 1.25×1.25 $\mu m^2$ to 2×2 $\mu m^2$ are open in the polyamide for $\alpha$-Si/Ag/Cu/Ag stack to contact $p$-Si. We do not observe, however, any dependence of probability and density of the Ag/Cu filaments in $\alpha$-Si on the window size. We also explore the effect of varying thicknesses of $\alpha$-Si and Cu layers while keeping the Ag layer intact, as the relative thicknesses of Ag and Cu may affect the endurance of the memristor [7].

### 2.2. Operation of the memristors

The newly fabricated memristors have a high resistance in the G$\Omega$ range. The noticeable conductance appears when a bias voltage, typically larger than 5 V, is applied, see Fig. 2 *a*. The transition is step-like; the current increases by almost 6 orders of magnitude, from nA to mA. At higher bias, the curve has several up/down current steps. The negative bias below 4 V resets the device to a high resistance state.

The memristor circuit can be modeled as a chain of elements in sequence: the metallic Ni/Au electrode with an ohmic contact to heavily doped $p$-Si, the insulating $\alpha$-Si, and the metallic Ag/Cu/Ag/Al top contact. The phenomenological model of the device elaborated in [15] nicely fits an experimental $I$–$V$ curve; see the dashed curve in Fig. 2 *b*. The model was developed for the metal–$TiO_2$–metal structure. It takes into account a time-dependent threshold bias voltage, nonlinear ion diffusion, and electron tunneling. A set of the fitting parameters is given in Table 1. The threshold switching voltage in the model, $V_p$, of 5.0 V is close to what was observed in the experiment. The different resistance states developed by programming pulses are likely a result of the ion motion in the Ag/Cu filament formed in $\alpha$-Si. With an increasing number of programming pulses, the arrangement of the ions in the filament is stabilised, so it becomes harder to alter the resistance states [16]. In the model, this corresponds to the saturation of the state variable at the boundary [15].

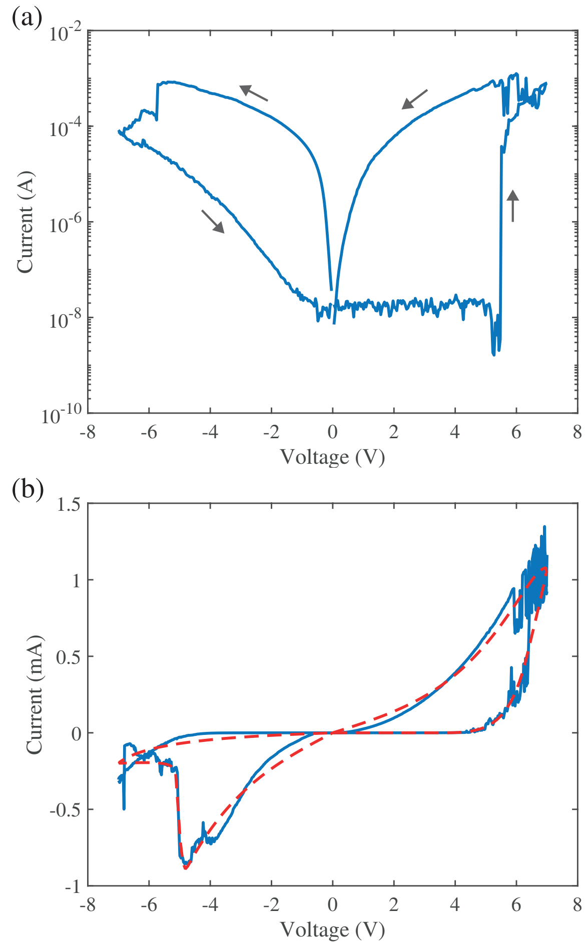


**Fig. 2.** Current–voltage characteristics of the $\alpha$-Si memristor. *a* — The electroforming *I*–*V* curve of a fresh memristor. Conductive Ag/Cu channels are formed in $\alpha$-Si when the bias voltage exceeds 5 V. The state relaxes back to high resistance when the negative voltage is applied. *b* — Approximation of the electroforming curve with the generalised model, shown with a dashed curve [15]. The fitting parameters are given in Table 1

**Table 1.** Calculated fitting parameters according to the phenomenological model presented in [15]. $\alpha_p$, $\alpha_n$, $w_p$, and $w_n$ determine when the motion of a state variable is no longer linear and to which degree it is dampened; $A_p$ and $A_n$ show the speed of ion motion; $V_p$ and $V_n$ represent threshold voltages for positive and negative biases, respectively; $a_1$ and $a_2$ are related to the thickness of the dielectric layer; $b$ determines the non-linearity of *I–V* characteristics; $w_0$ is the initial value of a state variable; $f(\mathbf{p}^*)$ is the final residue value of the fitting parameters $\mathbf{p}^*$

| $\alpha_p$ | $\alpha_n$ | $w_p$ | $w_n$ | $A_p$ | $A_n$ | $V_p$ |
|---|---|---|---|---|---|---|
| 1.10 | 13.42 | 0.017 | 0.57 | 0.33 | 3.11 | 5.06 |

| $V_n$ | $a_1$ | $a_2$ | $b$ | $w_0$ | $f(\mathbf{p}^*)$ |
|---|---|---|---|---|---|
| 4.60 | 0.19 | 0.31 | 0.39 | 0.04 | 0.77 |

There are a limited number of distinct states that memristors may take on in response to voltage pulses, Fig. 3 *a*. The switching between the resistance states is rather stochastic, but negative pulses predominantly decrease conductivity and may even reset the memristor to its original high resistance state. To alter the resistance state, we apply square voltage pulses from 1 V to 7 V of various durations, from 50 ns to several seconds; Fig. 3 *b*. There is a little effect if pulses shorter than 100 ms are applied. It may be explained by the slow dynamics of the Ag/Cu ions in $\alpha$-Si. A somewhat similar threshold effect is observed with the amplitude of the pulse. A noticeable effect starts with pulses larger than 1 V; see Fig. 3 *b*, inset.

Despite the stochastic nature of resistive switching, the states are stable over time, Fig. 4. It takes some time for the resistance to relax to a stable value after the programming pulses. The relaxation time is varied among the memristors in a wide range of $\tau \approx$100 *ms*–1000 *s*. There is a correlation between the relaxation time and the duration of the voltage pulse; a shorter pulse results in faster relaxation. However, we did not find any consistency in the relaxation time across different memristors.

The thickness of $\alpha$-Si is one of the limiting parameters of the memristor. We observed stable multi-state switching in $\alpha$-Si with thickness ranging from 6 to 9 nm. It is consistent with the results of other experimental groups [7].

We have also investigated the transport properties and switching behaviour of the Ag/Cu filament in $\alpha$-Si

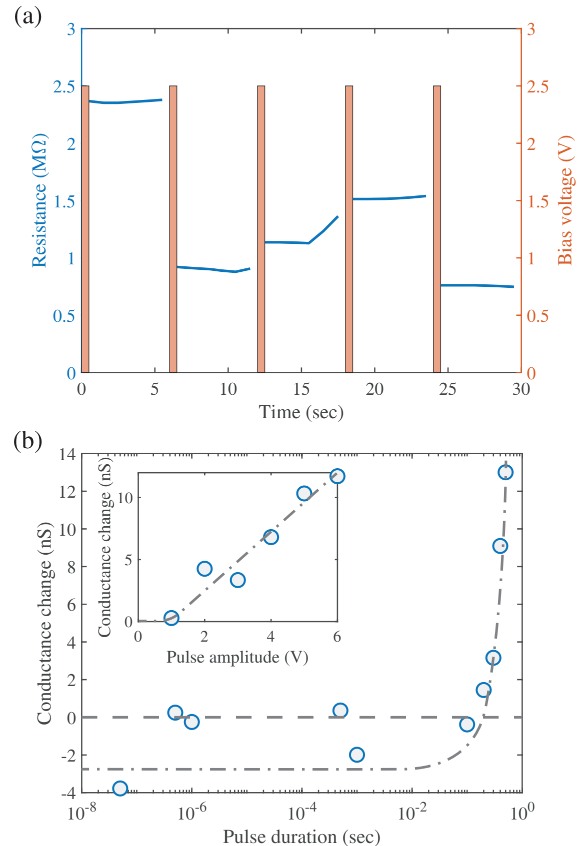


**Fig. 3.** Response of pre-formed $\alpha$-Si memristors to short voltage pulses. *a* — Change of the resistance with a sequence of programming pulses 5 V/0.5 s (red bars). *b* — The threshold nature of the programming with the pulse duration or pulse amplitude (inset). The conductance changes when pulses longer than 0.1 s and larger than 1 V are applied

at low temperatures down to 150K. The conductivity at temperatures above 220 K can be modeled by the activation of the electrons in the extended states of $\alpha$-Si by $\sigma = \sigma_0 \exp\{(-E_a/kT)\}$, where activation energy $E_a$ = 0.1 eV, Fig. 5 [17]. We also observed that the switching voltage decreases with rise in temperature, suggesting that Joule heating may play a role in both the formation and rupture of the channel, Fig. 5, inset.

### 2.3. Analysis of 3×3 memristor crossbar array

At low bias, the $I$–$V$ curves of memristors are non-linear. The non-linearity can be characterised by the ratio of current at the bias voltage $V$ and that at $V/2$ [14]. For our memristors, the ratio reaches 12. The non-linearity limits the size of the usable memristor crossbar array because of the parasitic sneak-path cur-

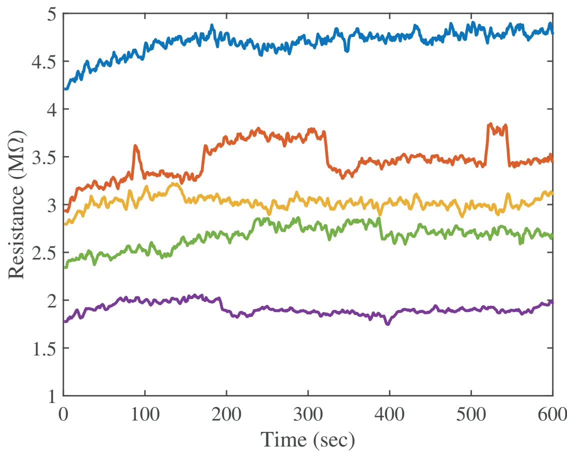


**Fig. 4.** Variation of resistance of a single memristor demonstrating the relaxation and retention of the memristor after the programming pulse

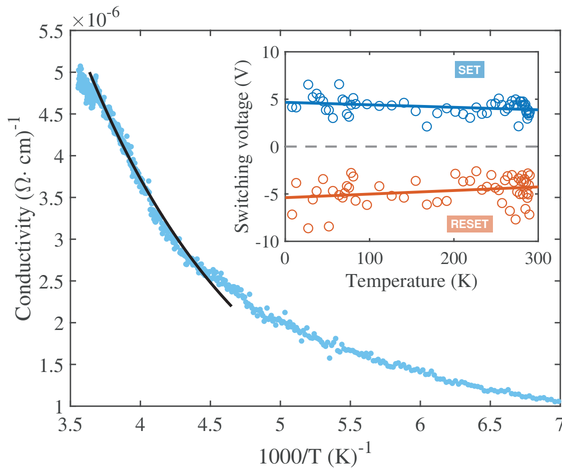


**Fig. 5.** Temperature dependence of the memristor conductivity in a temperature range from 285 K to 150 K. The solid black line is a fitting curve assuming the activation energy $E_a = 0.1$ eV. Inset: distribution of set and reset voltages in a wide temperature range

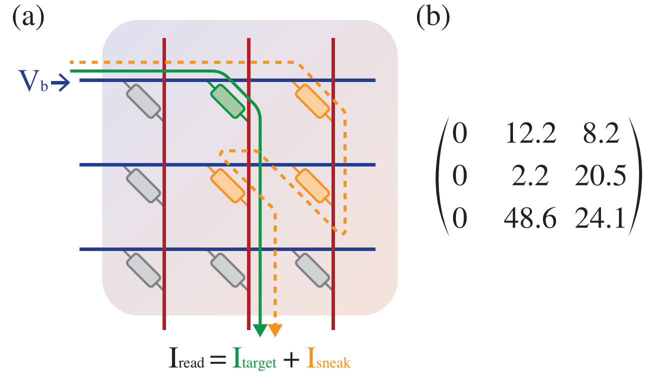


**Fig. 6.** Utilisation of a 3×3 crossbar array of memristors for vector-by-matrix multiplication. *a* — Sneak-path current in the memristor crossbar array. The current flows not only through the target cell ($I_{\mathrm{target}}$), but also through the neighbouring cells ($I_{\mathrm{sneak}}$). *b* — Matrix with the node weights. The weights are conductances normalised to 2 nS for convenience

**Table 2.** The vector-by-matrix multiplication

| vector | (1 1 1) | (1 1 0) |
|---|---|---|
| prediction,nA | (0 62.9 34.2) | (0 14.3 10.2) |
| measurement,nA | (0 49.5 24.0) | (0 13.0 8.6) |
| rel.dev., % | (0 21.3 29.8) | (0 9.1 15.7) |

| vector | (1 0 1) | (0 1 1) |
|---|---|---|
| prediction,nA | (0 60.7 32.2) | (0.2 50.7 26.1) |
| measurement,nA | (0 49.5 32.3) | (0.1 49.5 23.8) |
| rel.dev., % | (0 18.5 0.3) | (0 2.4 8.8) |

rents, which alter the weight of the matrix nodes when the input load to the matrix lines changes; see Fig. 6 *a*. The parameters of our memristor allow us to design a crossbar array of 10×10. For the demonstration, we explore a smaller crossbar array of 3×3. Here, the 3-memristor-long and 5-memristor-long sneak-path currents should be taken into account [18].

We programme memristors with 5 V pulses and probe the states with 0.5 V pulses for 500 ms. In what follows, we use conductance instead of resistance for the state of the nodes. After the initial programming, the memristors have conductances ranging from 4.4 nS to 97 nS. We normalised them to 2 nS for convenience and presented them in the form of a matrix of weights in Fig. 6 *b*. One should mention that these values contain the effect of sneak-path currents when the bias is applied to the wordline of the corresponding node. We would expect that the weight would change if several input signals are applied to the crossbar array simultaneously. The memristors at the left-most bitline are in the high-resistance state; thus, their conductance is taken as 0. The current flowing across them is below the noise level of our measurement system.

We exploit the crossbar arrays by applying voltage signal to only one or to few wordlines. In the former instance, we have the following input vectors (1 0 0), (0 1 0) and (0 0 1), where «1» corresponds to 0.5 V and «0» to 0.0 V. This method allows us to get the weights in the matrix, Fig. 6 *b*. An expected output current for the vector-by-matrix multiplication with this

weight matrix at the $j$-th bitline is $I_j = \sum_{i=1}^{3} V_i G_{ij}$, where $V_i$ is an input voltage to the $i$-th wordline and $G_{ij}$ is the conductance of the node at the $i$-th wordline and $j$-th bitline. We compare these results with the that when the other vectors are at the input: (1 1 1), (1 1 0), (1 0 1), and (0 1 1). The readings and relative deviation (rel.dev = $(|I_{\text{pred}} - I_{\text{meas}}|)/I_{\text{pred}}$) are shown in Table 2. The difference between the values can be as high as 30%. It is due to the effect of sneak-path currents combined with the non-linear conductance of the memristors, $G_{ij}(V) \neq const$. We should note that the sneak path currents are eliminated when we send the vector (1 1 1) [18]. Another possible reason of the deviation is the fluctuation of $G_{ij}$'s with time.

## 3. CONCLUSION

We fabricate and explore individual memristors and crossbar arrays of memristors. The memristors have switching non-linear $I$–$V$ characteristics when the programming voltage greater than 2 V is applied. It is a consequence of the Ag/Cu filamentation in the thin $\alpha$-Si layer, which brings the resistance of the memristor to the M$\Omega$ range. We can alter the resistance state with voltage pulses above 2 V and durations longer than 100 ms. We have combined memristors into a 3×3 crossbar array and performed vector-by-matrix multiplication. The sneak-path currents and arbitrary fluctuations of the resistance state result in an 87% accuracy of the operation.

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